Substitute Specification

ABSTRACT OF THE DISCLOSURE

The electronic data processing circuit targets the emulation of a logic function. The circuit includes a single clock providing time unit signals, a programmable synchronous logic array for processing values on a time unit basis, detection of internal or external value state changes known as events , programmer for state changes or event signals, processor for a series of scheduled times providing the logic array with scheduled time signals depending on the signals from the detection or the event programmer and the signals from the clock. The processor can determine subsequent scheduled times having delayed deadlines programmed by the programmer, depending on the signals from the detection or the programmer. The processing performed by the logic array is thus dependent on the series of scheduled times triggered by internal or external value state changes and by determination of the series of scheduled times.